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(54) Subscribers loop synchronisation

(57) In a PCM system, it is desirable for the two ends to remain in synchronisation, and for this purpose both channel associated and non-channel associated synchronisations are used.

The PCM code combinations are eight bit codes, each with a ninth bit for sync and a tenth bit for data. When sync search is in progress, either at switch on or after sync has failed, the seventh and eighth bits of the PCM code bits are used to convey additional sync, thus reducing the risk of simulation. To locate the sync all other bits except the sixth and tenth bits are set to zero, the sixth and tenth bits being at one. Thus we get two ones separated by five zeros, which is a pointer used to locate the sync. The sync is located by storing a data frame on reception and shifting it to find the combination of two ones separated by five zeros. The shift needed to find the combination indicates the extent of misalignment and is used to bring the clock into alignment with the incoming bit streams.

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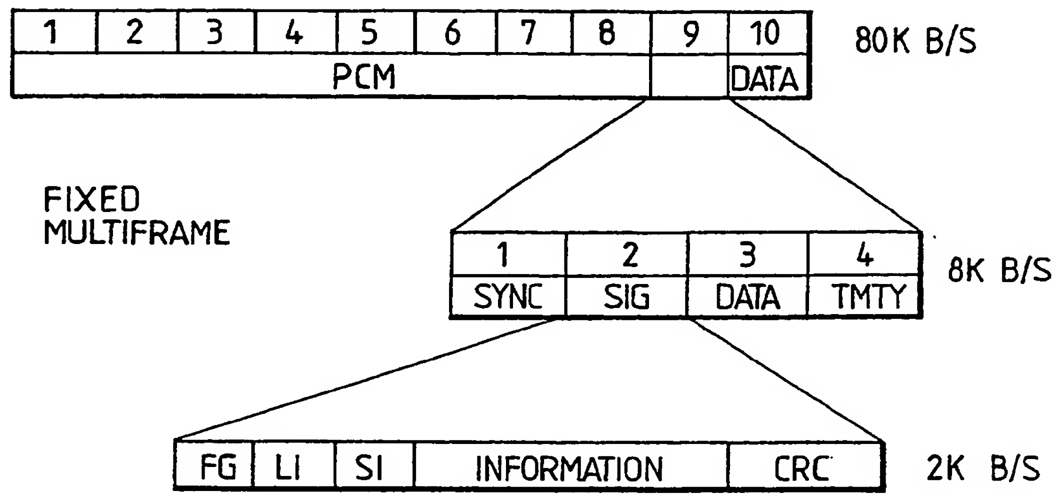


Fig.1

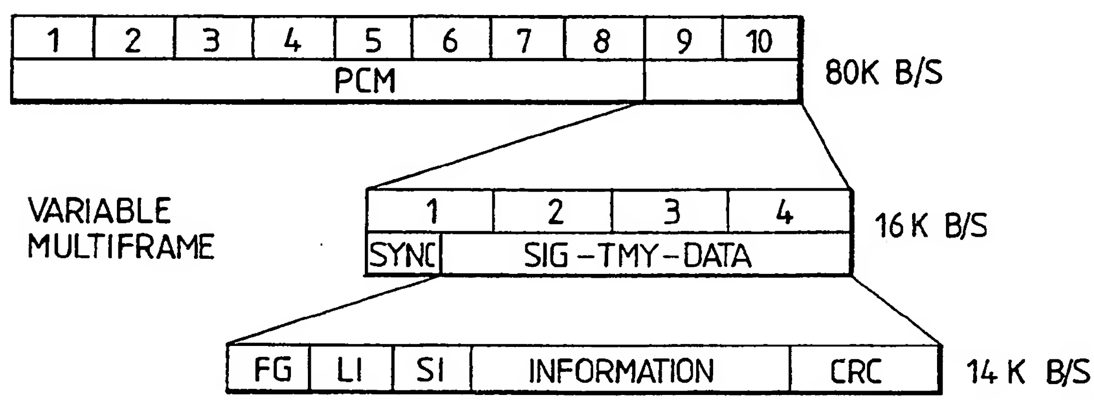


Fig.2

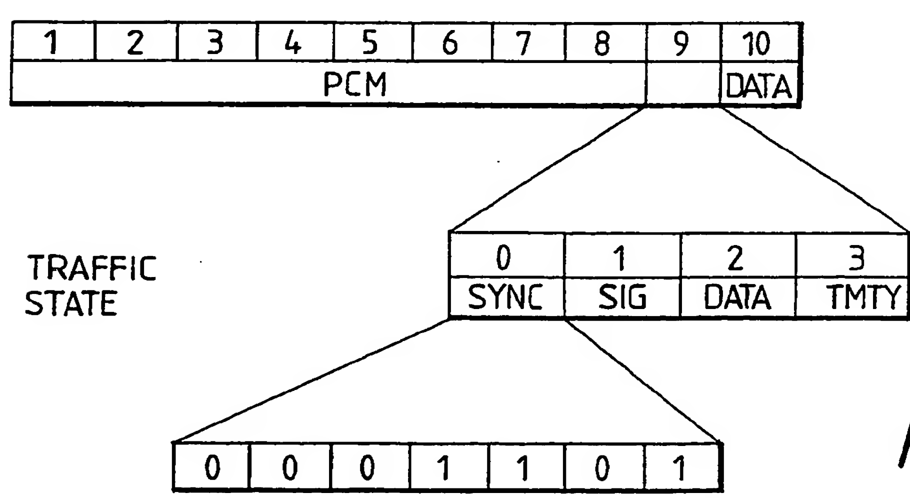


Fig.5

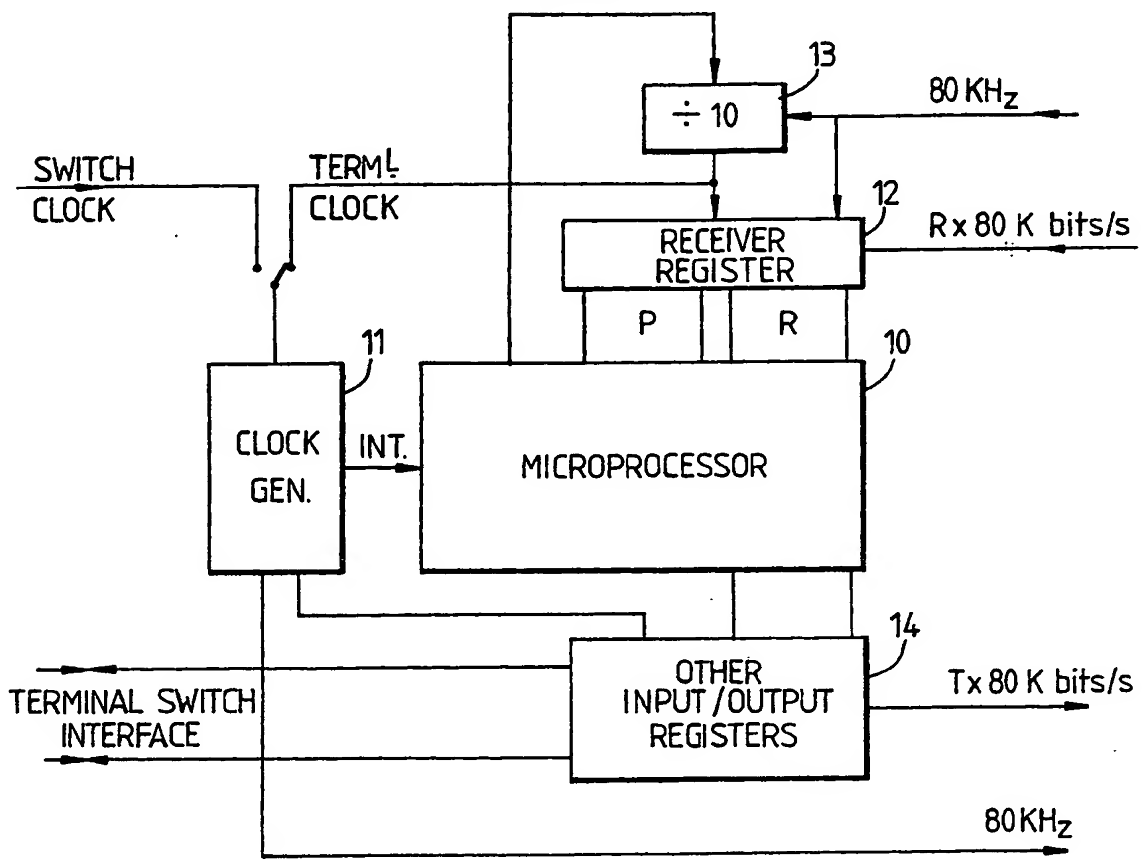

13
÷ 10
80 KHz
SWITCH
CLOCK
TERMl.
CLOCK
12
RECEIVER
REGISTER
Rx 80 K bits/s
P
R
11
10
CLOCK
GEN.
INT.
MICROPROCESSOR
14
OTHER
INPUT / OUTPUT
REGISTERS
Tx 80 K bits/s
TERMINAL SWITCH
INTERFACE
80 KHz

Fig. 3

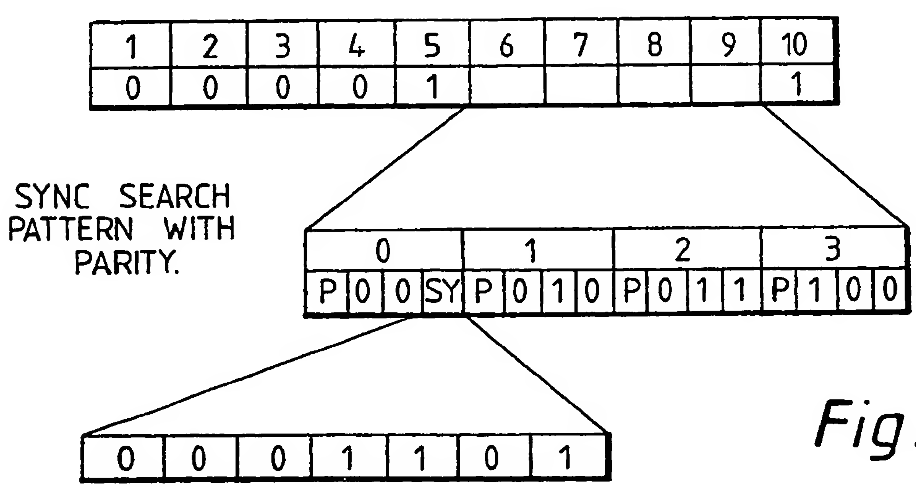
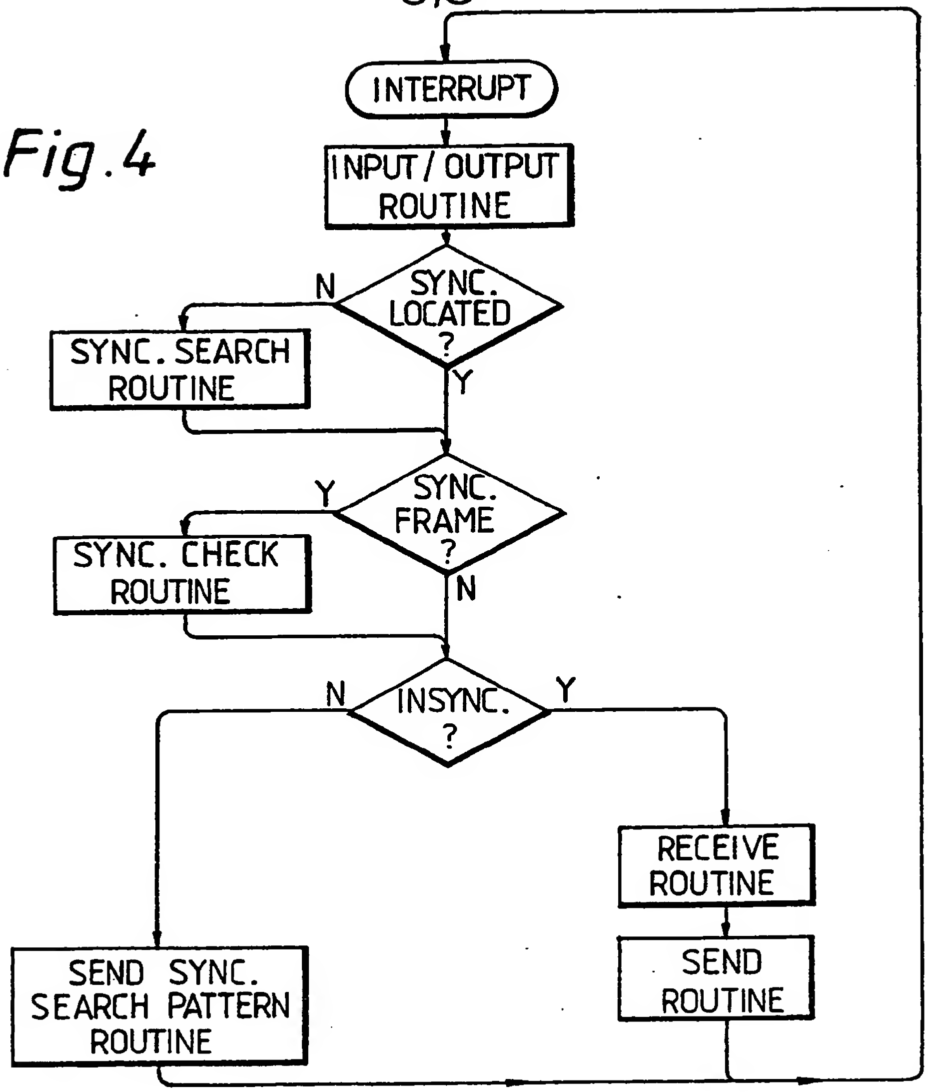

1 2 3 4 5 6 7 8 9 10
0 0 0 0 1 1
SYNC SEARCH
PATTERN WITH
PARITY.
0 1 2 3
P 0 0 SY P 0 1 0 P 0 1 1 P 1 0 0
0 0 0 1 1 0 1

Fig. 7

Fig.4


INTERRUPT
INPUT / OUTPUT ROUTINE
SYNC. LOCATED ?
N
Y
SYNC. SEARCH ROUTINE
SYNC. FRAME ?
Y
N
SYNC. CHECK ROUTINE
INSYNC. ?
N
Y
RECEIVE ROUTINE
SEND ROUTINE
SEND SYNC. SEARCH PATTERN ROUTINE

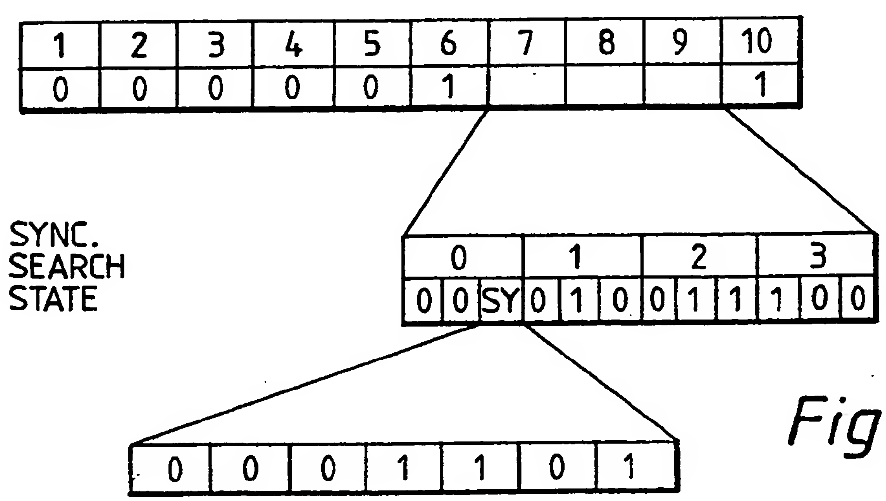

1 2 3 4 5 6 7 8 9 10
0 0 0 0 0 1 1
SYNC. SEARCH STATE
0 1 2 3
0 0 SY 0 1 0 0 1 1 1 0 0
0 0 0 1 1 0 1

Fig.6

SPECIFICATION

Subscribers loop synchronisation

This invention relates to telecommunication systems of the fully digital type, and especially to arrangements in such systems for providing that synchronisation between the subscriber's terminal and the system node or switch to which that terminal is connected.

In such a system voice, data and signalling information are transmitted in a multiplexed digital bit stream, using the well-established 8 bit PCM digitisation extended to give, for example, an 80kb/s bit stream. On reception at a receiver, either at a terminal or at a system node or switch, it is necessary to determine bit, frame and multiframe timing. To check synchronism, a synchronising pattern is sent within the multiframe, which usually embraces four ordinary frames. It is desirable to rapidly synchronise on switch-on and to rapidly resynchronise during receiving from synchronisation failure.

One proposed method is to initially send a synchronisation signal using the full baseband band width until synchronisation is attained, and then to revert to the normal synchronisation pattern in a multiframe time slot. This has disadvantages due to the need to switch from one synchronisation system to another. A second proposed method is to send the normal synchronisation pattern in the multiframe but with all other bits at zero during the synchronisation acquisition period: this has limitations in certain implementations, especially in noisy conditions which may cause extended time being needed to achieve synchronisation.

An object of the present invention is to provide a method of and apparatus for achieving synchronisation which is more rapid and simpler than those hitherto used.

According to the invention there is provided a digital PCM transmission system, in which the intelligence to be conveyed is handled in bit frames each of which can include an x bit PCM code combination, an $(x+1)$th bit usable, inter alia, for conveying synchronisation information and at least an $(x+2)$th bit usable for conveying other intelligence, in which when a synchronisation search occurs, either on switching the system on or in response to the loss of synchronisation, a plurality of y adjacent bits including the xth bit place, of the bits normally used for PCM, are used to convey synchronisation information, in which in each bit frame used to convey synchronisation information during a synchronisation search the $(x+2)$th bit and the bit preceding said plurality of adjacent bits are both set to a first binary condition with all other bits normally used for PCM set to the second binary condition, so that the pattern sent during synchronisation search includes two bits in the first binary condition separated by $(x\text{-}y)$ bits in the second binary condition, on which on reception of the bit stream sent during synchronisation search a complete frame of said bit frames is stored in a buffer store, in which the stored bits are tested for the presence of the combination of two bits in the first condition separated by $(x\text{-}y)$ bits in the second condition, in which the received bits are shifted under clock pulse control until the said combination is detected and the extent of the shift needed to detect that combination is noted, and in which the clock is adjusted in accordance with the said extent of shift to bring the clock into alignment in respect of alignment with the bit stream.

An embodiment of the invention will now be described with reference to the accompanying drawings, in which:

Figures 1 and 2 show two known bit multiplex arrangements for the use of the bits in the bit stream.

Figure 3 is a simplified block diagram of a system embodying the present invention.

Figure 4 is a basic flow diagram for synchronisation acquisition in a system such as that of Fig. 2.

Figures 5, 6 and 7 show synchronisation search patterns usable in a system such as that of Fig. 3.

The synchronisation system to be described is intended to determine and control the alignment of the received bits to ensure that digit integrity is maintained, to determined the alignment of the received frame and to identify frames within the multiframe. The system must provide for the initial detection of synchronisation in both directions of the subscribers's loop during call set-up, the monitoring of synchronisation during the call, and the recapture of synchronisation after failure during the call. The last should be achieved within the capabilities of common error detection systems, and preferably without interfering noticeably with speech.

The synchronisation pattern has to be so chosen that it is easily generated, easily detected, not unduly noise-sensitive, not easily simulated by traffic and should permit rapid recovery from loss of synchronisation. During initialisation the transmitted pattern should permit synchronisation to be found quickly and unambiguously.

The arrangement to be described herein was designed for use in 10 bit interleaved systems, in which there are four frames in a multiframe, an example of the bit arrangement for which is shown in Figs. 1 and 2, but is applicable to other bit interleaved systems of more than 10 bits and more than four frames. It is also applicable to other more advanced systems. In Fig. 1, in each word bit 10 is used to provide a data channel and bit 9 is used to provide several functions. Thus in the frame 1 of four frames of a multi-frame it is used to provide a data channel and bit 9 is

used to provide several functions. Thus in the frame 1 of four frames of a multi-frame it is used to provide synchronisation, in frame 2 it is used for signalling, in frame 3 for another (and slower) data channel and in frame 4 for telemetry.

The signalling involves the use of at least two multi-frames or, in effect, a super-multi-frame, the allocation of the bits in these frames being as follows in the present case:

(a) bit 1, FG, is a flag bit-set in successive frames to 0's and 1's so as to define a byte 01111110, which indicates that a signalling word is present.

(b) the next bits, LI, are used to indicate length, i.e. how many frames are embraced by the signalling word.

(c) next bits, SI, form a service indicator, e.g. an address to be used for the signalling word.

(d) then there is a block of bits labelled INFORMATION, used to convey the signalling information.

(e) a frame check sequence CRC, usable in checking frame alignment and in checking for the presence of data bit errors.

An alternative use of the ninth and tenth bits is shown in Fig. 2: here bits 9 and 10 are used together so that the four-frame multi-frame gives a 16 kb/s channel, of which bit 1 is used for synchronisation in alternate channels, bits 2, 3 and 4, plus bit 1 in alternate channels, giving a 14 kb/s signalling channel the bit allocation of which is as for the signalling channel of Fig. 1.

The "hardware" used in the present system includes a micro-processor 10 shown functionally in Fig. 3. The synchronisation search program is started by an interrrupt signal provided at regular time intervals by a clock generator 11. This occurs one per frame, since it is not practicable for the interval to be as a bit period, as that does not permit a sufficient number of processor instructions between interrups.

The received 80 kb/sec line signal is entered into a sixteen bit serial/parallel register 12 under control of an 80KHz clock pulse train, as shown. This clock pulse train is divided in a divide-by-ten circuit 13 to give a received frame clock train. The line signal passes from the register 12 into the micro-processor 10 as a sixteen bit sample. When this is correctly synchronised the first byte consists of a PCM octet, while the first two bits of the second byte are the additional bits (bit 9 and 10, Fig. 1 or 2) used to make up the ten bit frame. The remaining six bits in the word are bits 1–6 of the next frame, and have no function in respect of the current frame.

In normal operation in the "traffic" state, each PCM octet is immediately transferred to an output register in the block 14, but during the sync. search state, all sixteen bits in the register 12 are examined for a synchonisation pattern–see below. Registers with accommodation for the entire 80k bit/sec of a frame of transmitted traffic, including voice traffic, are loaded or read once per frame, and registers for other traffic or signalling are serviced by the micro-processor at the appropriate rate. These registers are included in the block 14.

Fig. 4 is an executive level flow diagram for the microprocessor program.

We now refer back to Fig. 3, to consider bit, frame and multi-frame synchronisation. The received 80 kbit/sec bit stream is isochronous with the terminal's transmitted timing. A bit rate clock is recovered from the incoming bit stream in well known manner, and applied via the connection shown to the microprocessor 10 and the divider 13. This clock is used, as shown, to enter the incoming bit streams serially into the register 12, and the register contents are read by the microprocessor in response to its interrupt. Thus provided that an "interlock" is arranged to prevent the register from being up-dated during read-out it is not necessary to re-align bits.

The output from the divider 13 provides a frame clock, which is used to staticize the incoming information in the register. However, for that information to be meaningful the phase of the frame clock needs to be aligned by the synchronisation signals. This is achieved by presetting the divider appropriately.

The microprocessor operates on a "per-frame" basis, but needs to be able to identify the frame within the multi-frame. This is achieved by aligning a frame counter to the frame contaning the synchronisation signal.

We now describe synchronisation search with special reference to Figs. 5 and 6. When the system is out of sync. it is necessary to transmit a signal to enable sync. to be found, which signal is referred to herein as a synchronisation search pattern (SSP). The SSP includes the same synchronisation pattern as is used in normal transmission, so as to avoid complications when changing from the Sync. Search Routine to the Sync. Check Routine (used in the "in-sync" state). Further, SSP does not include any traffic since that would serve no useful purpose and would confuse the detection system. In fact, any traffic bits would, when out-of-sync, be scrambled.

Thus the simplest form of SSP is sync + zero, i.e. the sync pattern in its normal position, bit 9 in the appropriate PCM word in frame 0 of the multiframe, and all other time slot bits at zero. This has the disadvantage that since only 1 in 40 bits are sync bits and only about half of them are bits, it can be relatively long time, e.g. 2ms, before a sync bit is detected, and a further period, e.g. 4ms, is needed to check the sync pattern. In a noisy environment many false detections may occur, each detection having to be checked

with the sync pattern, which extends the time needed for a true detection of sync several fold. Further, the sync-check itself may fail due to an error in the sync, pattern, causing a false rejection or requiring the check to take place over several sync pattern intervals.

In the present system, sync detection during sync search is improved by using the bandwidth normally occupied by traffic. The additional sync information needed consists of a pointer to the location of the sync bit, the identity of the frame within the multiframe, and the identity of the multiframe within the sync pattern sequence. Ideally this information should be contained within a single frame.

In the present system there are four frames in a multi-frame, so the identities of the frame of the multiframe can be encoded using two bits. As the ninth bit is used for sync, see Fig. 5, the two bits to provide this coding are placed in the seventh and eigth bit position when in the sync search state, see Fig. 6. Bits 7, 8 and 9 together provide for eight combinations, two of which can occur in the sync-frame of the multi-frame, as the sync-bit (the ninth) can be 0 or 1. Thus six identifiable combinations can be allocated to the non-sync frames, which gives a maximum capability of seven frames per multiframe.

In a word being considered in a given frame, the seventh, eigth and ninth bits can be of either polarity so their location is only identifiable if they have a unique pattern. The resulting ten-bit word must form a cyclically permutable code, and must not be degenerate, i.e. must only appear once in any ten bits of repeated sequence. These criteria are satisfied by setting the sixth and tenth bits of the word to 1, see Fig. 6. This shows the utilisation of bits seven to nine during sync search, plus the sixth and tenth bits at 1.

During the sync search process, a complete frame of information is entered into the microprocessor, but its orientation with respect to the processor word is not known. Hence the search process shifts, i.e. rotates, its contents until two 1 bits are located five bits apart with all zeros between them. The amount of shift needed to achieve this is a measure of frame displacement and is used to preset the frame clock divider. Frame synchronisation is acquired under control of this at the next entry. The frame identity can also be read and stored in the microprocessor memory, and incremented at each interrupt.

In a noisy environment, there is a probability of locating two 1 bits five bits apart, one of which is erroneous. This would give a false detection of sync, which would be rejected later but would waste time. However, testing the bits between the two 1's for zero enables such an error to be detected and the sync attempt to be aborted.

An error in the seventh, eigth and ninth bits gives a false frame identity, so the sync pattern is sought in the wrong frame. Thus sync-check fails, with the resultant time penalty. Thus it can be shown that with a bit error rate of 1 in 10^3, 1 in 3,600 sync attempts fail for this reason. This can be avoided by the use of an extra bit for parity, e.g. by using bits six to nine for sync search purposes, in which case the sync pointer bits are now four bits apart, and there are two such combinations in the frame, i.e. the cyclic code is degenerate. If odd parity is used this difficulty is resolvable but it needs extra processor instructions. The value of parity in this case is thus a matter of a "trade-off" in the prevailing error environment. In systems with 11 or more bits per word, there is no penalty involved including parity, which is then a useful addition.

The microprocessor system operates satisfactorily with any synchronisation code, but a pseudo-random polynomial has advantages as it is easily generated and detected, either in hardware or in software. Further, although it is difficult to simulate, in traffic, it is very quickly identified to be correct or incorrect. The shortest produced pseudo-random sequences is (2^3-1), i.e. 0001101. Another useful synchronisation pattern is the 15 bit sequence (2^4-1). Either of these can be readily generated using feedback shift register arrangements.

CLAIMS

1. A digital PCM transmission system, in which the intelligence to be conveyed is handled in bit frames each of which can include an x bit PCM code combination, an $(x+1)$th bit usable, inter alia, for conveying synchronisation information and at least an $(x+2)$th bit usable for conveying other intelligence, in which when a synchronisation search occurs, either on switching the system on or in response to the loss of synchronisation, a plurality of y adjacent bits including the xth bit place, of the bits normally used for PCM, are used to convey synchronisation information, in which in each bit frame used to convey synchronisation information during a synchronisation search the $(x+2)$th bit and the bit preceding said plurality of adjacent bits are both set to a first binary condition with all other bits normally used for PCM set to the second binary condition, so that the pattern sent during synchronisation search includes two bits in the first binary condition separated by $(x-y)$ bits in the second binary condition, on which on reception of the bit stream sent during synchronisation search a complete frame of said bit frames is stored in a buffer store, in which the stored bits are tested for the presence of the combination of two bits in the first condition separated by $(y-x)$ bits in the second condition, in which the received bits are shifted under clock pulse control until

the said combination is detected and the extent of the shift needed to detect that combination is noted, and in which the clock is adjusted in accordance with the said extent of shift to bring the clock into alignment in respect of alignment with the bit stream.

2. A system a claimed in claim 1, and in which one of said *y* additional bits is a parity bit.

3. A digital PCM transmission system, in which the intelligence to be conveyed is handled as ten bit frames each of which can include an eight bit PCM code combination, a ninth bit usable, inter alia, for conveying synchronisation information and a tenth bit usable for conveying other intelligence, in which when a synchronisation search occurs, either on switching the system on or in response to the loss of synchronisation, two additional bits, the seventh and the eighth, of the bits normally used as part of the PCM code combination are set to their 0 state, so that the pattern sent during synchronisation search includes two 1 bits separated by five 0 bits, in which on reception of the intelligence sent during a synchronisation search a complete frame of ten bit words is stored in a buffer store, in which the stored frame is tested for the preserve of the combination of two 1 bits separated by five 0 bits, in which the received frame of ten bit words is shifted under clock pulse control in the buffer store until the said combination is detected and the extent of shift needed to find that combination is noted, and in which the clock is adjusted in accordance with the said extent of shift to bring the clock into alignment with the bit stream.

4. A digital PCM transmission system, substantially as described with reference to the accompanying drawings.

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